Optimized Hardware Realization of Digital Sigma-Delta Modulator for Integrated Frequency Synthesizers

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Frequency Synthesizer in Direct Conversion I/Q Transceiver

Scope of this Work

V. Solomko, TU Cottbus
Sigma-Delta PLL as a Frequency Synthesizer

Advantages of Sigma-Delta Frequency Synthesizers

Relaxed requirements to the reference oscillator:
• reference frequency must not be an integer multiply of channel center frequency (arbitrary choice of reference frequency);
• possible to compensate crystal frequency drift.

Drawbacks of Sigma-Delta Frequency Synthesizers

Signal purity degradation due to:
• spurious tones;
• quantization noise of sigma-delta modulator.
Sources of Spurious Tones in Integrated Sigma-Delta Frequency Synthesizers

Spurious Tones

Fractional

PLL Nonlinearities
Intermodulation
Tones in $\Sigma\Delta$ Modulator

Reference

Digital Noise Coupling
Mismatches and Leakage Currents in PLL

Implementation of digital sigma-delta modulator

Scope of this Work

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Choice of Sigma-Delta Modulator: MASH 1-1-1

Advantages

- unconditional stability;
- ease of integration;
- highly decorrelated output sequence;

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Tones in MASH 1-1-1 Modulator

Undithered modulator

Dithered modulator

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Dither Generator Implementation

Basic circuit of pseudo-random noise generator

Amplitude spectrum of supply current

- Dither period: $2^n/F_{ref}$;
- Additional all-zero detector circuit is required;
- Triggered by the $F_{ref}$, it produces digital noise amplitude spectrum of which has peaks at $F_{ref}$, $2F_{ref}$, ....
Digital Noise Coupling in Integrated Synthesizer

Performance degradation caused by digital noise coupling depends on:

- noise sources (divider, sigma-delta modulator);
- noise sensitive receptors (VCO, loop filter);
- coupling paths (substrate, supply lines).

Optimized hardware implementation of sigma-delta modulator reduces spurious caused by digital noise coupling

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Investigated Hardware-Optimized Dithering Topologies

### Direct feedback dithering

**Advantages**
- No additional hardware
- High-pass shaped dither

**Drawbacks**
- Tones at low frequencies
- Introduces DC component

### Oscillator-based dither generator

**Advantages**
- Good tone suppression
- Minimum additional hardware
- No DC component

**Drawbacks**
- No high-pass shaped dither
Oscillator-Based Dither Generator

- Carrier frequency of the free-funning VCO is not correlated with the reference frequency;
- Oscillation frequency is several times higher than the reference frequency;
- Wideband FM takes place: modulation index $m = \Delta f / f_{VCO} > 0.3$;
- Supply current does not have high-amplitude spikes repeating with period of reference frequency.

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Spectral Content of Dither Generated by the Oscillator-Based Dither Generator

Sigma-delta modulator

Modulated VCO

Quantized VCO signal

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Influence of Oscillator-Based Dither Generator on the Phase Noise

Oscillator-based dither generator does not degrade the phase noise of the PLL

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# Oscillator-Based versus Pseudo-Random Dither Generator (Simulation Results)

<table>
<thead>
<tr>
<th></th>
<th>Oscillator-based dither generator</th>
<th>10-bit pseudo-random generator</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Amplitude spectrum of supply current</strong> (reference frequency is 64 MHz)</td>
<td><img src="image1.png" alt="Graph" /></td>
<td><img src="image2.png" alt="Graph" /></td>
</tr>
<tr>
<td><strong>Current consumption</strong></td>
<td>54 μA</td>
<td>269 μA</td>
</tr>
<tr>
<td><strong>Occupied area</strong></td>
<td>180 μm²</td>
<td>378 μm²</td>
</tr>
</tbody>
</table>
**Fully Integrated 11 GHz Sigma-Delta PLL with Oscillator-Based and Feedback Dithering**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Infineon 0.12 μm RF-CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>50 mA</td>
</tr>
<tr>
<td>Reference Frequency</td>
<td>64 MHz</td>
</tr>
<tr>
<td>Locking Range</td>
<td>10.32 GHz – 11.2 GHz</td>
</tr>
<tr>
<td>Frequency Resolution</td>
<td>31.25 kHz</td>
</tr>
<tr>
<td>Reference Spurs</td>
<td>&lt; –66 dBc @ F_{ref}</td>
</tr>
<tr>
<td></td>
<td>&lt; –58 dBc @ 2F_{ref}</td>
</tr>
<tr>
<td>Fractional Spurs</td>
<td>&lt; –70 dBc @ 70% locking range</td>
</tr>
<tr>
<td>Phase Noise (bandwidth: 1 MHz)</td>
<td>–80 dBc/Hz @ in-band</td>
</tr>
<tr>
<td></td>
<td>–140 dBc/Hz @ noise floor</td>
</tr>
<tr>
<td>Occupied Area</td>
<td>1000 μm x 800 μm</td>
</tr>
</tbody>
</table>
Spurious Tones with Different Dithering Topologies

PLL output signal with direct feedback dithering

PLL output signal with oscillator-based dither generator

**NOTE**: Displayed span is 45 kHz

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Spurious Tones Caused by PLL Nonlinearities

**NOTE**: Displayed span is 20 MHz

Spurs caused by nonlinearities are independent on whether the oscillator-based or direct feedback dithering is used

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PLL Phase Noise

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Conclusions

• An empirical study of two hardware-efficient dithering topologies for digital sigma-delta modulators were presented;
• Direct feedback dithering requires no additional hardware, however, some low frequency, low power tones still exist;
• Oscillator-based dithering generator offers good tones suppression while having lower supply current spikes, lower current consumption and smaller occupied area than conventional pseudo-random generator;
• Oscillator-based and direct feedback dithering topologies do not degrade the phase noise of the PLL;
• Both dithering topologies can be used in high-frequency, low power, low cost integrated frequency synthesizers.