Bachelor/Master Thesis:

Design and Implementation of a Decoder within a 10-bit DAC used in a Front-end Transceiver Enabling Ethernet in Automotive

Digital-to-analog converters are one of the fundamental blocks of analog front-end transceivers to transfer the digital data into analog signals on the channel. The transceiver is targeting for the first 1Gbit/s standard and beyond for automotive industries. One of the critical parts of DAC design, is the binary to binary/thermo decoder which a smart design of it is essential for a high performance DAC.

This work targets to study and implement this decoder in a 28 nm technology.

Goals:

1) Study the state of the art within segmented decoders.
2) Design and implementation of at least two segmented decoder to compare.
3) Study different performance parameter of each decoder alone.
4) Simulating at different corners to verify functionality of the design at worst cases.
5) Top level simulation with a model of the 10-bit DAC to test the effect of the dynamic behavior of the DAC and effect of the decoder in it.

Stretched Goals

6) Layout the decoder with 28 nm technology.

What you learn:

1) Simulation and Implementation with Cadence Virtuoso.
2) In depth understanding of mixed signal circuit design.
3) In case of layout, learning to use layout XL.

What you need to know before:

1) Basic understanding of analog circuit design.
2) Intro of cadence virtuoso (not a must)
3) Intro to layouting (not a must)

Contact: hossein.ghafarian@tu-berlin.de

27 Juni 2016