Bachelor/Master Thesis:

Crosstalk Cancellation Techniques for DDR5-SDRAM Data Buffer Frontend in 28nm CMOS Process

DDR-SDRAM is used as memory module in most laptops and personal computers. DDR4-SDRAM was introduced into market mid of 2014 with I/O frequencies ranging from 0.8 GHz up to 1.6 GHz. Developers are currently working on a standard for DDR5 to further increase memory performance, with frequencies up to 3.2 GHz (which translates into 6.4Gbit/s per lane).

Unfortunately, the physical characteristics of the mainboard as interface between CPU and RAM do not change, and at high data rates, the capacitive coupling increases. Thus, signals from adjacent wires on the board are coupled into the signal path and thus distorting the signal.

Fig.: DDR4-SDRAM, source https://de.wikipedia.org/wiki/DDR-SDRAM

Goals:
- Crosstalk research: study how transitions within one signal path affect the surrounding signal paths using a DDR5 channel model
- Research and compare different crosstalk cancellation methods, evaluating their applicability in the frontend
- Implement and verify the functioning of a suitable cancellation technique
- Implement and verify the functioning of another suitable cancellation technique, compare with the first one (optional)

Requirements:
- Basic understanding of analog integrated circuits
- Basic understanding of “Nachrichtentheorie”
- Fun in research
- Cadence experience (optional)

Contact: s.lehmann@tu-berlin.de, EN421, ☎ 341-25682