Analog Transmitter and Receiver Concepts for Wireless Chirp Communication at 2.44GHz

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- Analog/RF IC design engineer at Nanotron Technologies GmbH, Berlin
- Mainly responsible for transmitter and RF oscillator design of transceiver IC’s for wireless chirp communication at 2.44GHz
- Industrial experience with design of laser driver IC’s for fiber optic data communication at Infineon Technologies AG, Berlin
- Study at the Technical University of Ilmenau, Theoretical Electrical Engineering, Graduation in 1993

Jaro Stimma
- Analog/RF IC design engineer at Nanotron Technologies GmbH, Berlin
- Responsible for design of integrated analog receivers for wireless chirp communication at 2.44GHz
- Industrial experience with design of high speed integrated analog receivers for fiber optic application at Infineon Technologies AG, Berlin
- Study at Hamburg University of Applied Sciences, Graduation in 1998
Outline

1) Chirp Transmission
   - Chirp Transmission Technique
   - Transceiver IC Architecture

2) Analog Transmitter
   - Transmitter Architecture
   - Transmitter Design Concept
   - Transmitter Results

3) Analog Receiver
   - Chirp Basics
   - SAW Filter Characteristic
   - Chirp Signals in Analog RX
   - Nanonet TRX (RX Heterodyne Concept)
   - NanoLoc TRX (Zero IF RX Concept)
   - Measurement Results (Nanonet Vs. NanoLoc)
   - Practical Analog Design Aspects
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Chirp Transmission Technique (1)

- Use Chirp signals for radio transmission
- A chirp pulse is a frequency modulated pulse
- Operation within 2.44GHz ISM band

Up-Chirp in the time domain (roll-off factor 0.25)
- The spectrum is flat
- The power spectral density is very low
- Optimal BT product
Chirp Transmission Technique (2)

- This chirp modulation technique is called: **Chirp Spread Spectrum (CSS)**

**Upchirp = logical high in time domain**

**Downchirp = logical low in time domain**

Linear frequency modulation from $f_{\text{LO}} - B/2$ to $f_{\text{LO}} + B/2$

Linear frequency modulation from $f_{\text{LO}} + B/2$ to $f_{\text{LO}} - B/2$
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Transceiver IC Architecture (nanoLOC TRX)

- 2.44 GHz ISM RF TRX IC
- 0.13μm SiGe BiCMOS
- Modulation: Chirp Spread Spectrum (CSS)
- Two bandwidth modes: 80MHz/22MHz
- FDMA possible (22MHz)
- Several chirp durations: 0.5μs/1μs/2μs/4μs
- Max. data rate: 2MBps
- Low power TRX
- VDD from 2.3V to 2.7V
- $T_{\text{amb}}$ from -40°C to 85°C
- Package QFN 48
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Transmitter Architecture

- Direct conversion transmitter
- Fully differential topology
- 6bit-DAC: $f_s = 244\text{MHz}$
- Low pass filter: Butterworth, 5th order

- Quadrature modulation
- Power gain control circuitry
- Class AB power amplifier
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Low Pass Filter Design Concept (1)

Low pass filter (LPF) Butterworth 5th order:

Conversion to active leapfrog filter structure:

- Integration of R-DAC in first stage
- R and C process deviation: calibration of C, R keeps constant
- Using capacitor arrays $C_N$ with MOS switches
- Calibration RC oscillator frequency
Low Pass Filter Design Concept (2)

Discussion: two filters or integration in one for the two channel bandwidths?

- Chip area for two filter (I and Q): 0.67mm² -> No
- Chip area for one filter structure (I and Q): 0.45mm² -> Yes
- Splitting of capacitor array in two capacitor arrays: $C_N \rightarrow C_{N,1} \& C_{N,2}$

<table>
<thead>
<tr>
<th>channel BW</th>
<th>bandwidth selection</th>
<th>capacitor array</th>
<th>current consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B_A = 80MHz$</td>
<td>$f_{3dB,A} = 33MHz$</td>
<td>$C_N = C_{N,1}$</td>
<td>$2 \times 1.52mA$ (I and Q)</td>
</tr>
<tr>
<td>$B_B = 22MHz$</td>
<td>$f_{3dB,B} = 8.7MHz$</td>
<td>$C_N = C_{N,1} + C_{N,2}$</td>
<td>$2 \times 0.99mA$ (I and Q)</td>
</tr>
</tbody>
</table>
I/Q Modulation (1)

- **Digital controlled oscillator**
- Division by 2: generation of quadrature outputs $0^\circ$, $90^\circ$
- Gilbert cell mixers
- Mixer outputs are added in current domain
I/Q Modulation (2)

Design aspects for I/Q modulation:

- Achievement of linearity in mixer
  - Resistive emitter degeneration of bipolar stage at the baseband port
  - IM3 <-44dBc

- Preventing from I/Q phase error
  - Identical layout for I and Q path
  - Short interconnections between divider-by-2-circuit and I/Q modulator
  - Post layout simulation with some iteration loops necessary

- Drive LO amplitude
Power Gain Control

- Programmable output power dynamic range: ≥ 33dB
- 6bit PGC register: 63 steps
- Low power design: Control of PA input signal amplitude in combination with control of PA bias current
- Gilbert cell based gain control implemented for amplitude control
- Programmable PA bias current with discrete current steps
Power Amplifier Design Concept (1)

**Power Amplifier (simplified):**

- **Matching and filtering circuitry:**

```
I_{bias2}  V_{bias1}
|     |     |
|     |     |
|     |     |
|     |     |
|     |     |

**Class A**

- L1: 3.9nH
- C1: 1pF
- L2: 5.6nH
- L3: 6.8nH
- C2: 3.3pF
- Balun: 200:50

**Class AB**

- V_{bias2} = 1.9V
- I_{bias1} = 1.9V

Ant. 50Ω
ESD concept at PA outputs:

- Two ESD diodes in series connected to VDD instead of one ESD diode as usual.

Passed ESD test conditions:
- Human Body Model: 2000V
- Charged Device Model: 500V
- Machine Model: 250V
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Transmitter Results (1)

TX output spectrum:

TX characteristics:
- Max. Pout = +2.5dBm @50Ohm SMA
- Max. PEP = +5dBm @IC output
- Dynamic range = 37.5dB
- -32dBr to f₀ ± 41.5MHz
- 2nd harmonic suppression: -56dBc
- 3rd harmonic suppression: -60dBc
- Carrier suppression: ≤-36dBc
- IDD analog = 23mA @ 80MHz
- IDD TRX = 33mA @ 80MHz
- IDD analog = 21.5mA @ 22MHz
- IDD TRX = 29mA @ 22MHz
- VDD = 2.3V ... 2.7V
Transmitter Results (2)

- Measurement results of power gain control:

![Graph showing typical TX output power at SMA connector and typical current consumption with PGC register value in dec.](image)

**Typical TX Output Power at SMA Connector**

- Measurement results of power gain control:

  - **Typical TX Output Power at SMA Connector**
    - Pout /dBm
    - PGC Register Value /dec

  - **Typical Current Consumption**
    - IDD total
    - IDD analog

![Graph showing typical current consumption with PGC register value in dec.](image)
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A chirp pulse is a frequency modulated pulse

Spectrum of the chirp pulse with bandwidth $B$ and a roll-off factor of 0.25

Up-Chirp in the time domain (roll-off factor 0.25)
A Simple procedure transforms the Chirp into a (Sinc-)Pulse
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SAW Filter for T=1\text{us} and BW=80\text{MHz}

**Group Delay Characteristic**

- UP – Channel
- DOWN - Channel

**Frequency Response**

- UP – Channel
- DOWN - Channel

<table>
<thead>
<tr>
<th>f [MHz]</th>
<th>220</th>
<th>250</th>
<th>280</th>
</tr>
</thead>
<tbody>
<tr>
<td>1\text{us}</td>
<td></td>
<td></td>
<td></td>
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</table>

Impact of the Test Environment

Statistical Data of 20 Components
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Chirp Signals in Analog RX 1

IF FM Signal
\[ f_{IF} = 250 \text{MHz}; \text{BW}_{\text{MAX}} = 80 \text{MHz} \]

IF AM Signal
\[ f_{IF} = 250 \text{MHz}; \text{BW}_{\text{MAX}} = 80 \text{MHz} \]

FM - / AM - Transformation
Chirp Signals in Analog RX 2

f_{LO}=f_{RF}=2,442\,\text{GHz}

RF FM Signal
(f_{RF}=2,442\,\text{GHz}; B_{W\text{MAX}}=80\,\text{MHz})

Zero IF Quadratur Downconversion

Baseband “FM – Signal”
(B_{W\text{MAX}}=40\,\text{MHz})
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Nanonet RX (Heterodyne Concept)

\[ f_{LO} = f_{RF} + f_{IF} = 2.692 \text{GHz} \]

\[ f_{RF} = 2.442 \text{GHz} \]

\[ f_{IF} = 250 \text{MHz} \]

Complementary Dispersive Delay Line DS1804C (CDDL)
Advantages of Heterodyne Nanonet RX

- Current Consumption of Chirp Correlator (SAW Filter) \( \rightarrow 0 \text{mA} \)
- Very Good IF BP Characteristic due to SAW Filter
- AC coupling in the IF circuitry possible (small C values)
- Low Flicker Noise due to IF
- Short RXON Settling time
- Relative Simple Analog AM-Chirp Detector
Disadvantages of Heterodyne Nanonet RX

- Constant Chirp BW and Chirp Duration because of SAW
- SAW Filter = External Component
- SAW – Driver required
- Image Rejection Aspect → ISM BPF
- Higher Current Consumption of IF Amplifiers
Heterodyne RX Design in 0,35um SiGe BiCMOS

- Full Differential Variable Gain LNA with LC Load
  - $I=4.5mA; NF=1.8dB@150\Omega; f_0=2.44GHz; BW=320MHz; Gain=12...26dB$;

- Full Balanced Gilbert Cell Mixer
  - $I=1.2mA; NF=5dB; Conversion Gain=15dB$;

- Full Differential AC Coupled Variable Gain Amplifiers
  - $I=1.6mA@BW=450MHz; f_0=250MHz; Gain=1...15dB$;

- AM – Chirp Detector with programmable detection threshold
  - $I=0.75mA$

- High Speed CMOS Comparator
  - $I=0.45mA$
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NanoLoc Receiver (Zero IF RX Concept)

RX RF

RX ANALOG BASEBAND (BW_{\text{MAX}}=40\text{MHz})

LO = RF = 2.442\text{GHz}

DIGITAL CHIRP CORRELATOR

VGA

ADC

LPF

VGA

LNA

IQ DEMOD

I

Q

0°

90°

Tx/Rx

R_{\text{RxP}}

R_{\text{RxN}}

RX RF (BW_{\text{MAX}}=80\text{MHz})
Advantages of Zero IF RX

- Variable Chirp Bandwidth and Chirp Duration because of programmable Digital Correlator
- No Image Rejection Filter
- No External Components (SAW) for RX necessary
- No Output Drivers
- Relatively Low BW of Baseband Amplifiers
- Digital AGC (because of ADC)
Disadvantages of Zero IF RX

- DC Offset Cancellation and RX Settling Time Aspect
- Flicker Noise
- Programmable Anti-Aliasing Filter required
- Higher Power Consumption of the Digital Chirp Correlator
- ADC Crosstalk Aspect → Power Supply Isolation
- High Layout Effort for Optimal Matching within the Circuitry
- Power Consumption and High Speed Vs. Large L – Values of CMOS Transistors in the Baseband Circuitry
Zero IF RX Design in 0,13um SiGe BiCMOS

- **Full Differential Variable Gain LNA with LC Load**
  - $I=4.5\text{mA}$; $\text{NF}=1.9\text{dB}$@200Ω; $f_0=2.44\text{GHz}$; $\text{BW}=225\text{MHz}$; $\text{Gain}=14..28\text{dB}$; $\text{Resolution}=2\text{dB}$;

- **Full Balanced Gilbert Cell Mixers**
  - $I=1.1\text{mA}$; $\text{NF}=4.8\text{dB}$@10MHz; $\text{Conversion Gain}=13\text{dB}$;

- **Programmable Differential Leap Frog Low Pass Filter (Butterworth 5th Order)**
  - see TX slides

- **Full Differential Variable Gain Amplifiers**
  - $I=0.2\text{mA}$@$\text{BW}=190\text{MHz}$; $\text{Gain}=1..15\text{dB}$; $\text{Resolution}=2\text{dB}$;

- **Full Differential Active High Pass Filters for DC Cancellation**
  - $I=500\text{nA}$@$f_{-3\text{dB}}=25\text{kHz}$;

- **Full Differential 5Bit Flash ADC**
  - $I_{\text{TOTAL}}=4.2\text{mA}$@0,28um CMOS; $\text{Sampling Frequency}=122\text{MHz}$; $\text{DR}=30\text{dB}$;
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# Measurement Results @ Nominal Conditions

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<tr>
<th>Electrical Parameters</th>
<th>Nanonet (Heterodyne RX) @ 0.35um SiGe BiCMOS ft,BIP=45GHz</th>
<th>NanoLoc (Zero IF RX) @ 0.13um SiGe BiCMOS ft,BIP=45GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption of Analog RX (Signal Path)</td>
<td>21mA</td>
<td>22mA *)</td>
</tr>
<tr>
<td>Current Consumption of Analogue RX incl. Freq.Synthesizer</td>
<td>27mA</td>
<td>28mA *)</td>
</tr>
<tr>
<td>Current Consumption of Complete RX</td>
<td>35mA</td>
<td>45mA</td>
</tr>
<tr>
<td>NF of RX @ incl. TX Load</td>
<td>3,0dB @ 150ohms</td>
<td>2,9dB @ 200ohms</td>
</tr>
<tr>
<td>NF of RX @ w/o. TX Load **)</td>
<td>2,4dB @ 150ohms</td>
<td>2,3dB @ 200ohms</td>
</tr>
<tr>
<td>IIP3 of analog RX **)</td>
<td>-17dBm</td>
<td>-9dBm</td>
</tr>
<tr>
<td>Voltage Supply Range</td>
<td>2.4V ... 3.6V</td>
<td>2.3V ... 2.7V</td>
</tr>
<tr>
<td>Ambient Temperature Range</td>
<td>-40°C ... +85°C</td>
<td>-40°C ... +85°C</td>
</tr>
</tbody>
</table>

*) ADC Design in 0.28um CMOS instead of 0.13um

**) Simulation Results
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Practical Analog Design Aspects

Concept of the LNA Input RX/TX Switch

Requirements:
- $R_{on} < 6\Omega$
- Good ESD Protection
- Low Parasitic Capacitance
Practical Analog Design Aspects

Realisation of the LNA input switch using an IO NMOS

Benefits:
- High ESD Protection
- Low Ron (Large W/L)

Drawback:
- Insufficient HF Model for IO NMOS
- High Parasitic Capacitance

(IO NMOS = NMOS with unsalicided drain and source area for good ESD protection)
Practical Analog Design Aspects

Realisation of the LNA input switch using a RF NMOS

(RF NMOS = NMOS with well RF model and bad ESD protection)

Benefits:
- High ESD Protection
- Well HF Model of the Switch Circuitry

Drawback:
- Additional High Ohmic Resistors for Drain- and Source – ESD protection required
- High Ron
- High Parasitic Capacitance
Practical Analog Design Aspects

Switches in Parallel for Low Ron Resistance Value

Benefits:
- Low Ron
- High ESD Protection
- Sufficient HF Model of the Switch Circuitry

Drawback:
- Large and Tricky Layout
Peak Over Mean - Chirp Detection (UP- or DOWN- Channel)

IF AM Signal

$f_{IF}=250\text{MHz}$;

$BW_{MAX}=80\text{MHz}$

IF Peak Detector

Mean Detector

Rectifier

RDAC

Comparator

TO DIGITAL

SIGNAL

THRESHOLD

Digital Baseband Signal
Practical Analog Design Aspects

Variable Gain Amplifier for Baseband Application

Good Experiences with Emitter Degeneration - Controlled Gain:
- Simple Programmable Emitter Degeneration
- Output DC Voltage independent of Gain
- Gain dependence on process variation very low
- Higher Linearity at Higher Input Level
- Simple Topology
Thank You!