Bachelor/Master Thesis:

Design and Implementation of a Tunable Bandgap Reference for a High-Speed, High-Resolution ADC

In analog-to-digital converters (ADCs) the conversion is performed with the assistance of a reference voltage which must remain constant at all times to prevent decision errors. This reference voltage can either be externally supplied or generated on chip via a bandgap reference.

In this work the bandgap reference for a state of the art 8GS/s SAR-ADC will be designed and implemented. The design has to be functional across corners and temperatures including mismatch variations. Furthermore, a correct startup has to be ensured. It is desired that the reference voltage is tunable. This thesis allows you to work with a modern 28nm CMOS technology.

Goals:
1) Familiarize yourself with standard designs of bandgap references
2) Build a bandgap reference in 28nm CMOS
3) Implement several features such as power down and a tunable output voltage

Stretch Goals:
4) Create the layout of the bandgap (mandatory for Master thesis)

Prerequisites:
Basic knowledge of analog circuit design
Experience with Cadence Virtuoso (AIC or AAIC knowledge is sufficient)

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