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Fakultät IV
Elektrotechnik und Informatik

Institut für Technische Informatik
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FG Mixed Signal Circuit Design

Institutsleitung
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Master Thesis:

Design and Implementation of a 12-bit 12 GHz Direct Digital Synthesizer in 22nm FDSOI

Direct Digital Synthesizer (DDS) is used for generating arbitrary waveforms with respect to the fixed frequency clock signal. The DDS we require here is used to feed the data into an RF-DAC. This work targets to study and implement the design in a 22 nm technology

Goals:

1. Design and Implementation of the circuit using VHDL/Verilog
2. Perform the synthesis
3. Perform the functional verification test
4. Place and Routing of the Design in 22nm
5. Power and Timing Analysis
6. Final Sign-off

Outcome of the thesis

Complete Digital ASIC Flow

Pre-requisites:

1. Basic knowledge of Hardware Description Language(HDL)
2. Basic Knowledge of Tool Control Language (TCL)

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