

04 Dezember 2018

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Fakultät IV  
Elektrotechnik und Informatik

Institut für Technische Informatik  
und Mikroelektronik

FG Mixed Signal Circuit Design

Institutsleitung  
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5. Dezember 2018

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## Bachelor/Master Thesis:

### Design and Implementation of 15-bit 1GHz Decimator design for Pipeline ADC in 65nm

Decimator is used to decimate an incoming signal from an ADC with two clock domain-crossing signals at a specified frequency

This work targets to study and implement the design in a 65 nm technology.

### Goals:

1. Design and Implementation of the circuit using VHDL/Verilog
2. Perform the synthesis
3. Perform the functional verification test
4. Place and Routing of the Design in 65nm
5. Power and Timing Analysis
6. Final Sign-off

### Outcome of the Thesis:

Complete Digital ASIC Flow

### Pre-requisites:

1. Basic knowledge of Hardware Description Language(HDL)
2. Basic Knowledge of Tool Control Language (TCL)

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